METHOD AND APPARATUS FOR SCANNING SEMICONDUCTOR WAFERS USING A SCANNING ELECTRON MICROSCOPE

FIELD OF THE INVENTION

This invention relates generally to Scanning Electron Microscope (SEM)-based scanning of specimens and, more particularly, to a SEM based method of scanning of semiconductor for defect inspection, and to a SEM-based method of scanning photo mask for defect inspection.

BACKGROUND OF THE INVENTION

Scanning methods of different kinds are used in applications that involve inspection of very small structures of objects in great detail. Some of these applications include defect review and inspection of specimens such as very large scale integrated (VLSI) circuits, wafers, or other articles, critical dimensioning of features in these specimens as well as design and process verification of the specimens. In such applications, scanning electron microscopes (SEM) are typically employed for scanning the specimens.

Scanning electron microscopes use an electron beam to scan the specimen. A SEM makes use of the wave nature of electrons to produce images with high resolution. A SEM operates by generating a beam of electrons called a particle beam. The particle beam is collimated by condenser lenses of the SEM and focused on the surface of the specimen through an objective lens system. The focused particle beam is deflected with the help of a deflection system of the SEM. The deflection system helps in moving the focused particle beam across the surface of the specimen in a particular direction for purposes of scanning. The deflected particle beam collides with specimen and generates secondary electrons (SE) and back-scattered electrons (BSE). The SE and BSE are then captured by a detector system of the SEM to produce an image of the specimen. The produced image is useful in inspecting the minute structures of the specimen under examination in great detail.

According to conventional SEM scanning methods for wafer inspection, the particle beam is first focused on the wafer and is then deflected either in parallel or perpendicular direction orientation with respect to the die orientation of the wafer. However, such a parallel or perpendicular direction of the deflected particle beam does not help in overcoming the edge effect or aliasing effect, which commonly occurs when scanning the patterned structures on a semiconductor wafer. Aliasing effect refers to the situation where the image lines appear to have jagged edges. During wafer scanning, aliasing may be caused by a slight misalignment between

the die orientation or the particle beam scanning direction, thus resulting in an apparent detection of non-uniformity along the edges of the patterned structure on the surface of the wafer by a detector system. This leads to an otherwise satisfactory wafer being categorized as faulty.

SUMMARY OF THE INVENTION

It is therefore a goal of the invention to provide a method in reducing the edge effect or aliasing effect in wafer inspections.

The aforementioned and related drawbacks associated with conventional SEM and methods of scanning specimens using a SEM are substantially reduced or eliminated by the present invention. The present invention is directed to a SEM, which scans the surface of a semiconductor wafer by performing the following steps: generating a particle beam from a particle beam emitter; and scanning the surface of the semiconductor wafer by deflecting the particle beam to a direction relative to the die orientation, such that the particle beam traverses a direction that is neither parallel nor perpendicular to the die orientation of the semiconductor wafer. According to the present invention, the particle beam is deflected onto the surface of the semiconductor so as to scan the surface of the semiconductor wafer at an angle within the preferred ranges of (1° and 89°) or (91° and 179°) or (-89° and -1°) or (-179° and -91°) with respect to the die orientation. According to the present invention, the SEM comprises: a particle beam emitter for emitting a particle beam in a SEM; and a deflective unit operative to scan the surface of the semiconductor wafer by deflecting the particle beam at an angle relative to the die orientation of the semiconductor wafer, such that the particle beam traverses a direction that is not parallel or perpendicular to the orientation of the die on the semiconductor wafer.

An advantage of the present invention is that the non-parallel and non-perpendicular scanning angles reduce aliasing effects.

Another advantage of the present invention is that the non-parallel and non-perpendicular scanning angles can be easily implemented with current scanning electron microscopes.

BRIEF DESCRIPTION OF THE DRAWINGS

The aforementioned and other advantages and features of the present invention will become better understood upon reviewing the following detailed description of the invention

taken in conjunction with the following drawings, where like numerals represent like elements, in which:

Figure 1 is a diagram illustrating a conventional semiconductor wafer having a plurality of die formed thereon;

Figures 2a and 2b are graphs illustrating a die orientation versus SEM scanning angle according to conventional methods of wafer scanning;

Figure 3 is an illustration of a particle beam being incidental on the surface of a specimen;

Figure 4a is a diagram illustrating an exemplary patterned structure on a semiconductor wafer;

Figure 4b is an illustration of the patterned structure showing aliasing effect in its image;

Figure 5 is a diagram illustrating a cross-sectional view of an embodiment of a scanning electron microscope in accordance with a preferred embodiment of the present invention;

Figure 6a is an illustration of a preferred embodiment of the present invention where the scanning direction vector lies at an angle within the range of 1° and 89° relative to the die orientation of the specimen;

Figure 6b is an illustration of a preferred embodiment of the present invention where the scanning direction vector is at an angle within the range of 91° and 179° relative to the die orientation of the specimen;

Figure 6c is an illustration of a preferred embodiment of the present invention where the scanning direction vector is at an angle within the range of -89° and -1° relative to the die orientation of the specimen;

Figure 6d is an illustration of a preferred embodiment of the present invention where the scanning direction vector is at an angle within the range of -179° and -91° relative to the die orientation of the specimen; and

DETAILED DESCRIPTION OF THE INVENTION

The SEM and method of operation thereof will now be described with reference to Figures 1 to 6d. Figure 1 is a diagram illustrating a conventional wafer **100** with a plurality of dies **105** formed thereon. In practice, each of the die **105** has electronic circuitries (not shown) formed thereon. The underlying circuitries are fabricated by a series of patterned structures of

interconnected lines (conducting and semiconducting) and interconnects formed on the surface of a semiconductor wafer. Each of these lines and corresponding interconnects of the circuitry is generally provided with either a parallel or perpendicular orientation with respect to the die orientation.

Figures 2a and 2b are graphs illustrating die orientation **110** versus SEM scanning angle **115** according to conventional methods of wafer scanning. Figure 2a illustrates the scanning angle **115** being perpendicular to the orientation of a die **120** on a semiconductor wafer. Figure 2b illustrates the scanning angle **115** being parallel to the orientation of a die **120.** This is according to conventional means of scanning employed in wafer inspection that require aligning the scan direction of particle beam **125** (shown in Figure 3) in a parallel or perpendicular orientation with respect to the die orientation **110** because integrated circuit structures are generally fabricated either in a parallel or perpendicular orientation with respect to the die orientation on a semiconductor wafer.

Figure 3 is a diagram illustrating a particle beam **125** being incidental on the surface of a semiconductor wafer **100** that is supported by a holder **124**. Conventionally, a SEM **140** comprises of a particle beam emitter **145** operative to emit a particle beam **125**. The particle beam **125** is passed across the surface of the semiconductor wafer **100** in either a parallel or perpendicular manner with respect to the die orientation as illustrated in Figures 2a and 2b respectively.

According to conventional wafer scanning methods, a slight shift in the orientation of the particle beam during scanning will result in the apparent detection of an irregularity along the edge of the patterned structure of the die on the semiconductor wafer **100** by a detector system **155**. During wafer inspection, this will result in an otherwise satisfactory wafer being categorized as flawed.

Referring now to Figure 4a, which shows an example of a typical patterned surface structure on a semoconductor wafer.

Figure 4b is an illustration of how aliasing negatively affects the image of the semiconductor wafer patterned structure provided by the detector system **155** correspond to the structure shown in Figure 4a. Aliasing occurs during scanning of the wafer and is caused by a slight misalignment between the scanning direction of the particle beam and the physical orientation of the patterned circuit structure on the semiconductor wafer surface thus resulting in

the detection of a non-uniformity along the edge of the surface patterned structure by the detector system **155.** Consequently, the resulting image displays jagged edges **250** along the patterned structure and causes an otherwise satisfactory wafer to be categorized as faulty.

Figure 5 is a diagram illustrating a cross-sectional view of an exemplary embodiment of a scanning electron microscope **140** in accordance with a preferred embodiment of the present invention. In this embodiment, SEM **140** comprises a particle beam emitter **145** (i.e., the effective source point for the particles) emitting a particle beam **125**, an anode **165,** an objective lens system **160** having a magnetic lens called a side pole lens composed of magnetic material **185** and exciting coils **190,** and a plurality of deflection units **175a-175e**. In a preferred embodiment, the particle beam is an electron beam and travels along a beam axis **180** between the particle beam source **145** and the semiconductor wafer **100**.. Typically, the specimen is a semiconductor wafer having feature sizes of about 0.05 μm to 0.20 μm or larger. An objective lens system **160** in the SEM **140** focuses the particle beam **125** into a small spot on the surface of the specimen, which is traversed over the semiconductor wafer **120** to be studied. The magnetic lens includes magnetic material **185** and exciting coils **190** for providing magneto-motive force to a magnetic circuit having field lines through the magnetic material and between the pole pieces **195** and **200**. The central bore of the magnetic lens has the shape of a circular bucket, which is axially symmetric about the beam axis **180**. At the place where the primary particle beam **125** enters the objective lens system **160**, through a beam-defining aperture **210**. The beam-defining aperture **210** determines the size of the particle beam **125** allowed to enter the objective lens system **160** and in one embodiment confines the beam diameter to about 0.1μm. A lens pole piece at the point where the primary particle beam **125** exits the magnetic lens is circumscribed by pole pieces **195** and **200.** A more detailed description of the SEM and its method of operation is present in co-pending patent application Serial No. 09/513,306 entitled "Swinging Objective Retarding Immersion Lens Electron Optics Focusing, Deflection and Signal Collection System and Method" and assigned to the assignee of the present invention is fully incorporated herein.

Immediately below the beam defining aperture **210** is an annular detector system **155** which collects secondary electrons (SE) and back scattered electrons (BSE) emitted from the semiconductor wafer **100** during the scanning operation. Detector system **155** has an aperture that is larger than the beam defining aperture **210** so the particles from the primary beam **125** are

not affected in any way by the detector system **155** as they pass through the beam defining aperture **210.**

Residing in the central bore are deflection units **175a-175d.** These units are disk-shaped rings, which are axially symmetric about the Z-axis. Located outside of the central bore is deflection unit **175e**, which is co-axial with the Z-axis and similar in construction to the deflection units within the central bore of the objective lens system. In accordance with the present invention, a first set of deflection units **175a, 175d** and **175e** deflect the particle beam spot a deflection field distance of about 600 μm in one version of the invention upon application of an appropriate voltage to the exciting coils **190**. A second set of deflection units **175b** and **175c** is dedicated to producing a more rapid scanning movement of the beam to cover an area of approximately 50 μm, and is centered on the position determined by the first set of deflection units **175a, 175d** and **175e**. Scanning is performed by dwelling on a point for a period of time (on the order of a few or tens of nanoseconds), moving to the next point in a row of points and then repeating the scan operation for the next row until an entire grid of points covering the area is scanned. If the beam spot rests at a position on the semiconductor wafer for 10ns then a single scan of a 50 μm line requires about 5 μs and the scan of the entire area takes at least 2.5 ms. In practice, an additional amount of time (about 1 μs/scan line) is required for retracing the beam between each successive scan causing the total time to scan the field to be about 3ms (2.5 ms + 500 × 1 μs). Deflection unit **175e** is particularly important for improving the size of the deflection field over the semiconductor wafer **100** because it is closest to the specimen and in the retarding field produced by the specimen. Thus deflection unit **175e** will have a large effect on the position of the particle beam **125** because it is deflecting a beam with much lower energy than the deflection units **175a-175d** and it is the deflection unit nearest the landing point of the beam on the specimen. On traversing across the surface of the semiconductor wafer **100**, the particle beam **125** is deflected by deflection units **175a – 175e** and captured by a detector system **155**. These captured electrons are called secondary electrons or back scattered electrons and are different from the primary electrons forming the particle beam **125** incidental on the surface of the semiconductor wafer **100**. Once the secondary electrons and the back-scattered electrons are captured by the detector system **155**, an image of the scanned semiconductor wafer is reconstructed. This image can then be used for wafer inspection to detect defects in the wafer in great detail.

Now referring to Figures 6a – 6d, according to the present invention, the scanning direction vector S used is neither parallel nor perpendicular to the die orientation on the surface of the semiconductor wafer. This is achieved by deflecting the particle beam at an angle in any of the ranges not including 90°, 180° or 270°. In accordance with preferred embodiments of the present invention, scanning angles within the ranges of (1° and 89°) or (91° and 179°) or (-89° and -1°) or (-179° and -91°) relative to the die orientation vector Dx are used. In accordance with the present invention, the preferred ranges of scanning angles are (15° and 75°), (105° and 165°), (-105° and -165°), (-15° and -75°)

Figure 6a is an illustration of a first embodiment of the present invention where the scanning direction vector S 116 lies at an angle within the range of 1° and 89° relative to the die orientation of the semiconductor wafer.

Figure 6b is an illustration of a second embodiment of the present invention where the scanning direction vector S 117 is at an angle within the range of 91° and 179° relative to the die orientation of the semiconductor wafer.

Figure 6c is an illustration of a third embodiment of the present invention where the scanning direction vector S 118 is at an angle within the range of -89° and -1° relative to the die orientation of the semiconductor wafer.

Figure 6d is an illustration of a fourth embodiment of the present invention where the scanning direction vector S 119 is at an angle within the range of -179° and -91° relative to the die orientation of the semiconductor wafer.

Anti-aliasing is the name for techniques designed to reduce or eliminate aliasing in the image of a surface structure on a semiconductor wafer. As discussed earlier, aliasing is caused by a slight misalignment between the particle beam scanning direction and resulting in the detection of an apparent irregularity along the edge of a surface structure on of the semiconductor wafer. By scanning the surface of the semiconductor wafer at an angle within the preferred ranges as provided above, the negative effects caused by aliasing are minimized thus producing images with much better quality along the edge of a structure.

Whereas the present invention may be embodied in many forms, details of a preferred embodiment are schematically shown in Figures 1 through 6d, with the understanding that the present disclosure is not intended to limit the invention to the embodiment illustrated. While the invention has been particularly shown and described with reference to certain embodiments, it

will be understood by those skilled in the art that various alterations and modifications in form and detail may be made therein. Accordingly, it is intended that the following claims cover all such alterations and modifications as fall within the true spirit and scope of the invention.